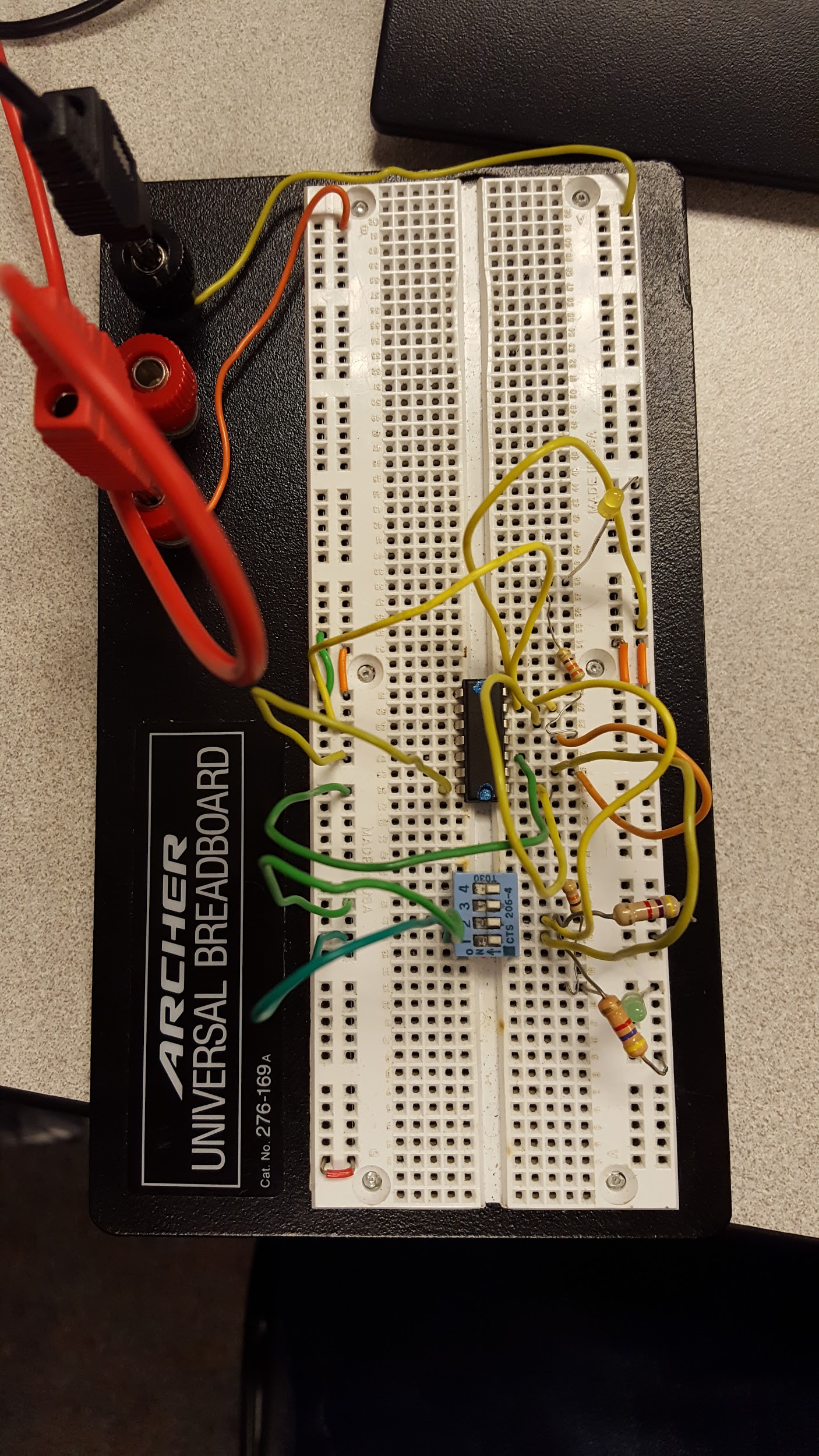
Hayden Miedema and Conner Toney

CIS 451-20  
Professor Kurmas

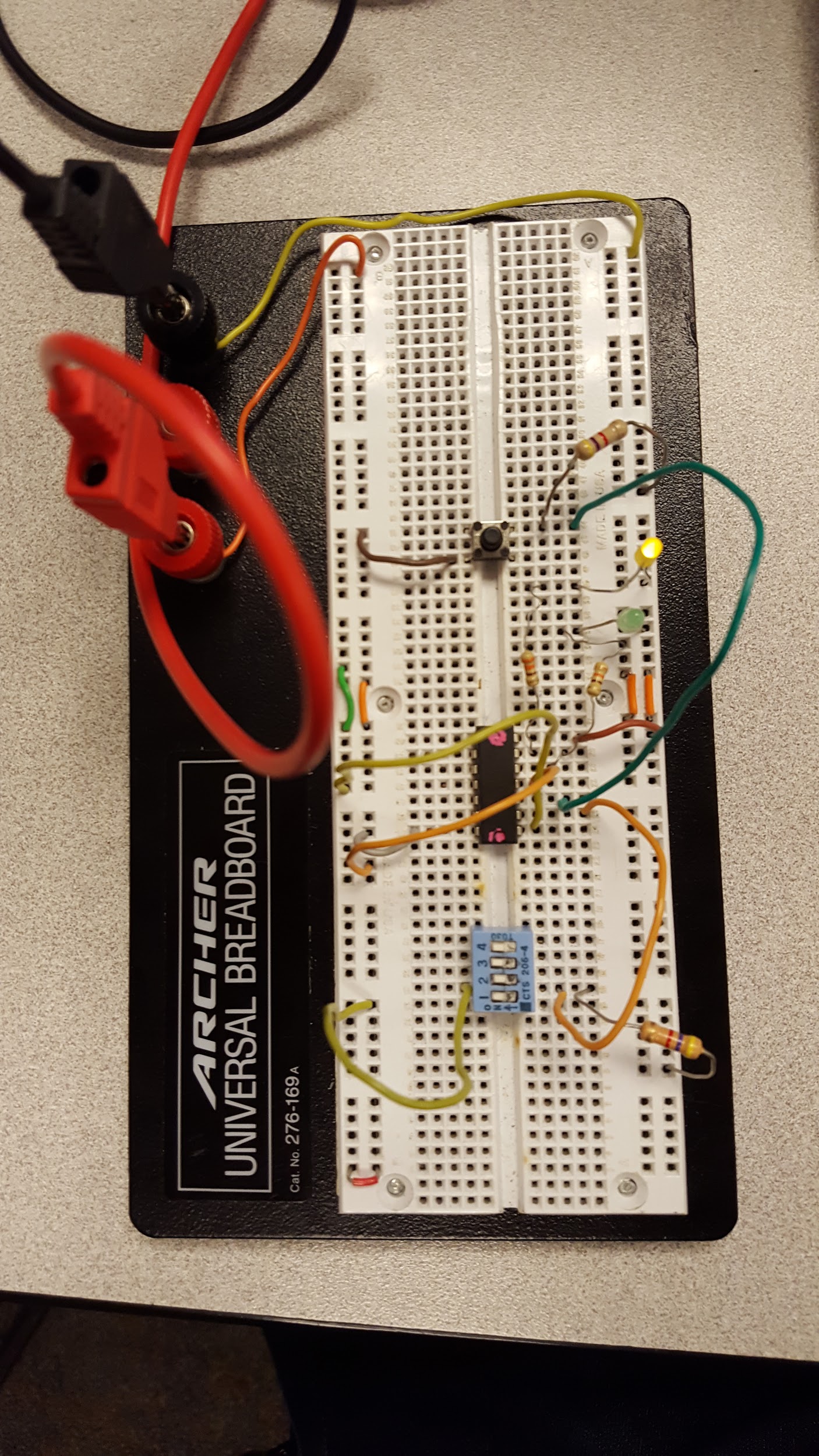
Lab 3: Introduction to Sequential Circuits

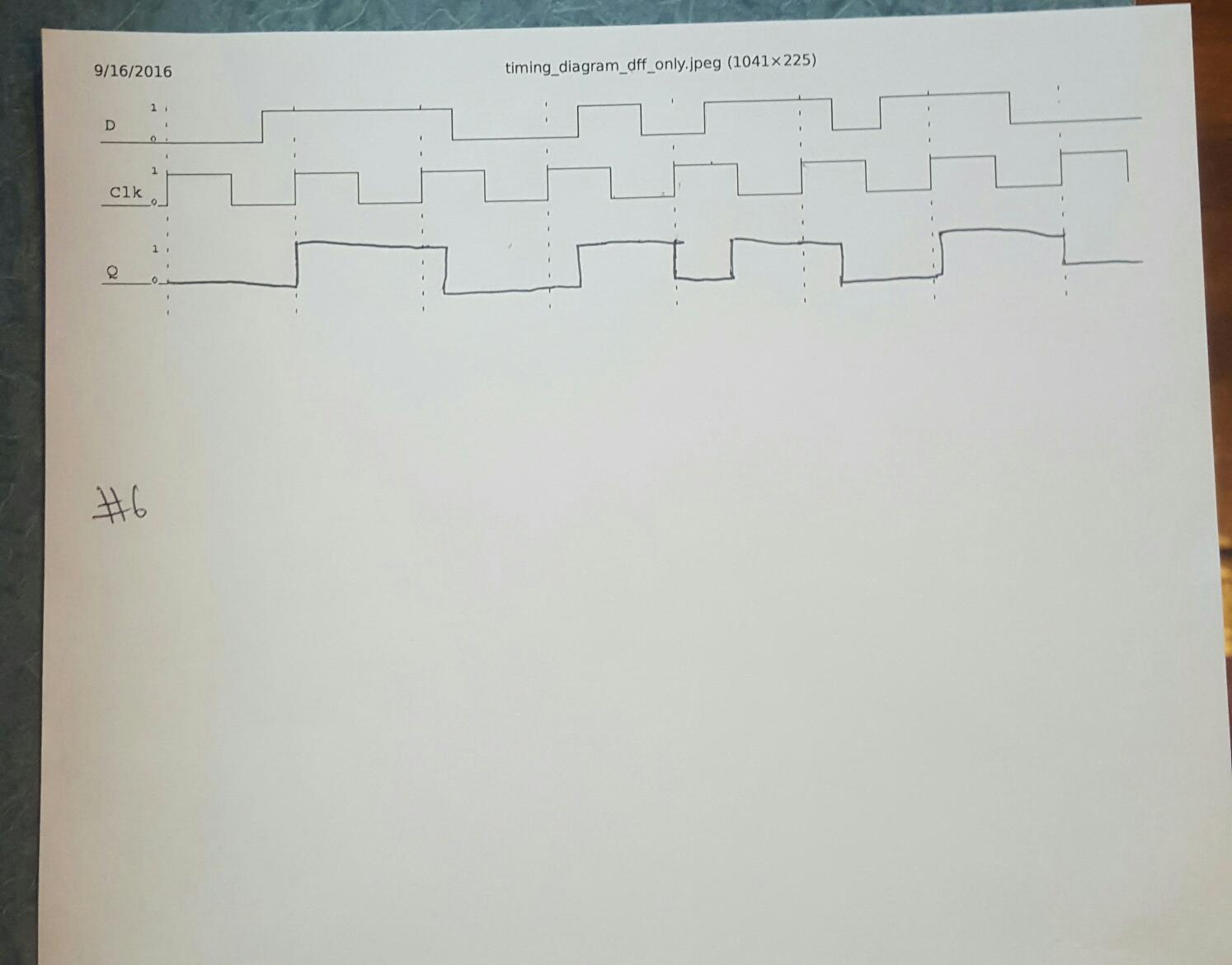
1. 
2. Notice that, unlike the combinatorial circuits we've discussed in class, the output of the S-R latch depends on both the inputs, and the current state of the device. A *characteristic table* is used to specify the output of the device in terms of both its input and current state. Determine, by observing the state of the LEDs, the characteristic table of the device.

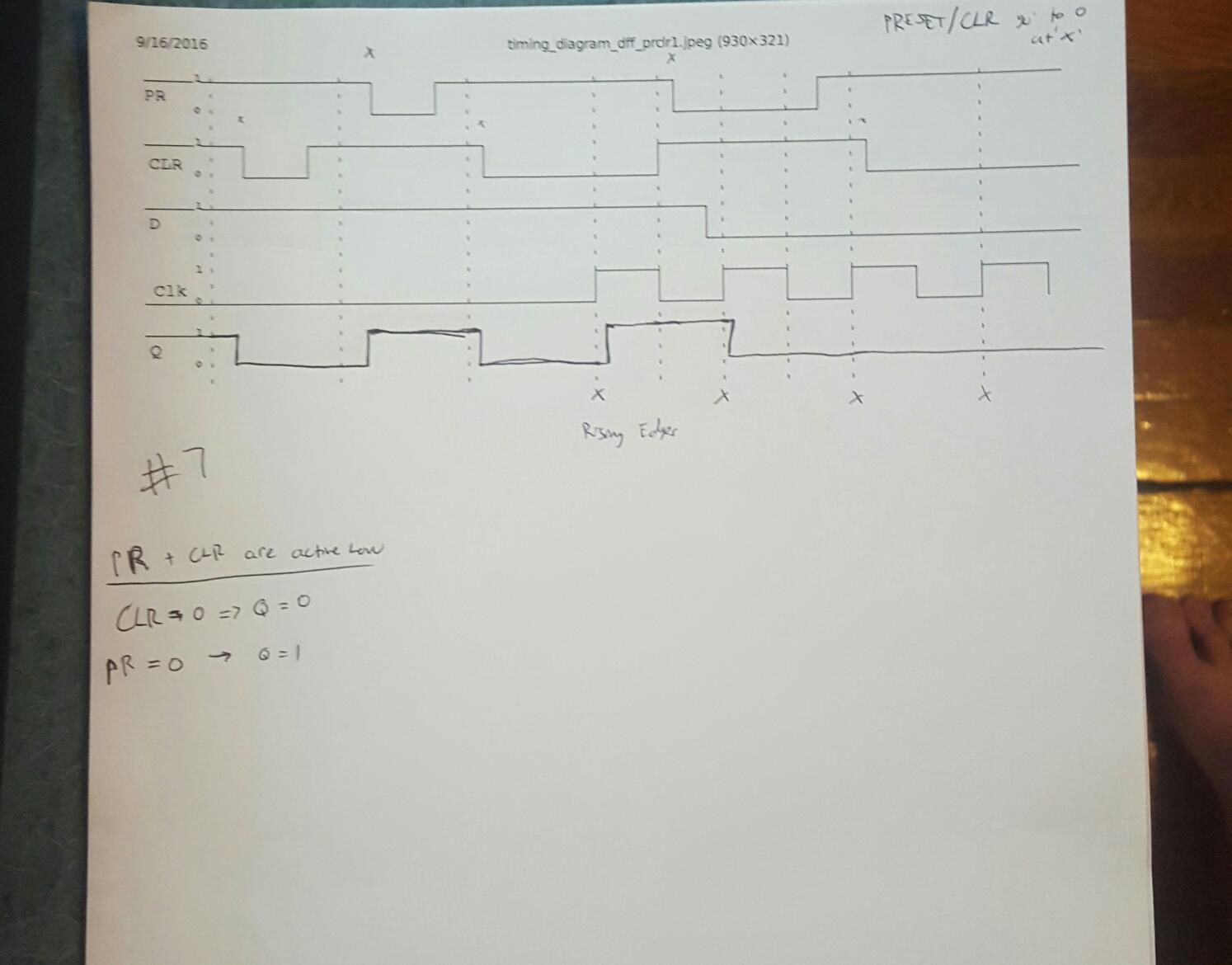
|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **R** | **S** | **previous Q** | **New Q** | **New Q'** |
| 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 1 | 0 | 0 |

1. They both output 0’s.
2. When R and S are both 1, the previous Q will not matter because sending a 1 into a NOR gate will output a 0 regardless of the other input. This then guarantees the “New Q’” to output a 0. This essentially doesn’t matter once again because the other input, ‘S’, is also a 1. These two will enter the NOR gate on the bottom of the diagram and output a 0 for the New Q value.
3. This state could happen if both Q and not-Q outputs begin in the same state. Then, the invalid condition is unstable when S and R are inactive, but when they start receiving input the circuit generally stabilizes due to one gate almost always reacting at a different speed than the other. If somehow both of the gates were exactly identical in receiving the inputs they would then oscillate between high and low without reaching a state of stability.

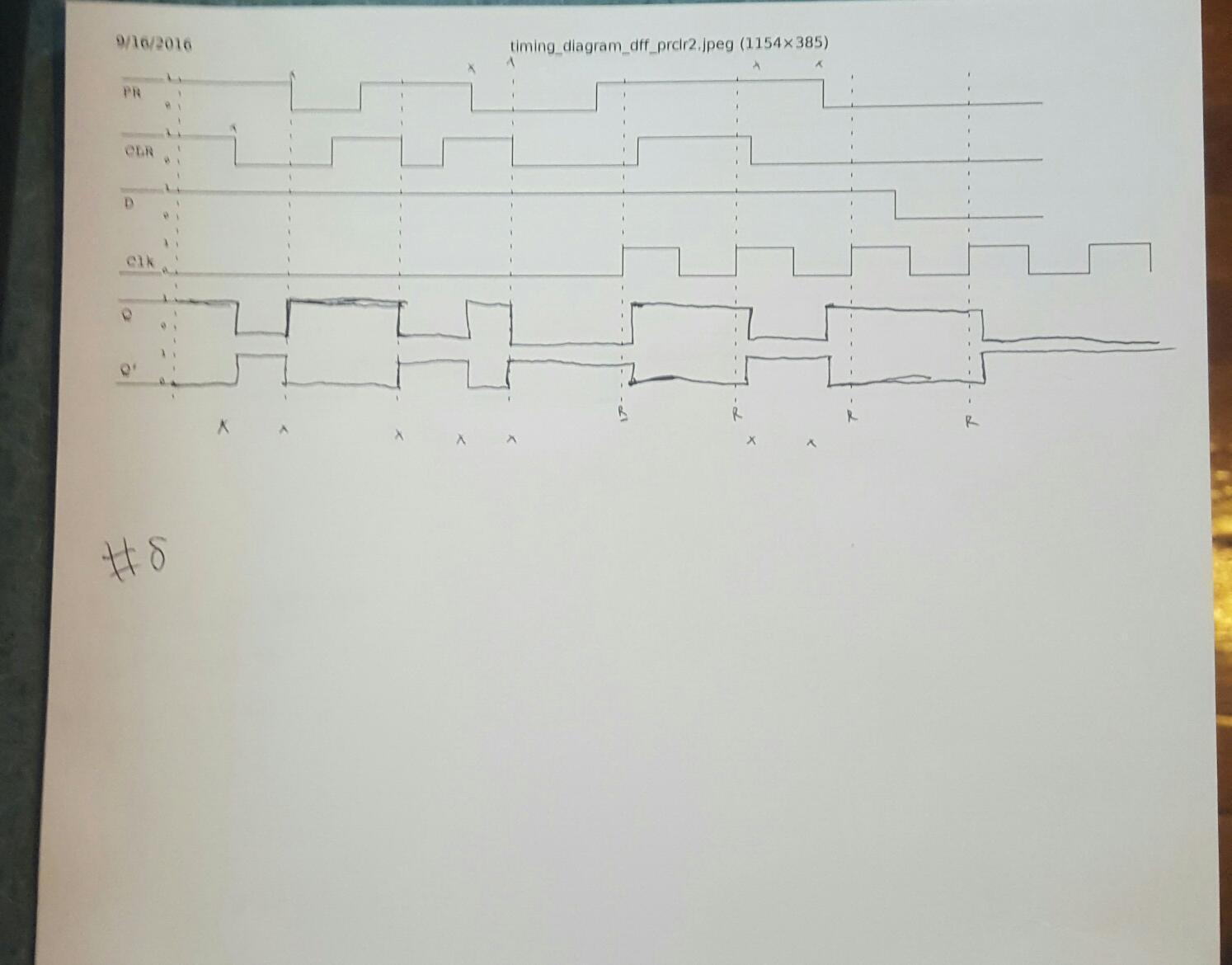
(this is the d flip flop with working clock)



1. 







|  |  |  |  |
| --- | --- | --- | --- |
| A1 Before | A0 Before | A1 After | A0 After |
| 0 | 0 | 0 | 1 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 0 |

1. We created a counter that increments.
2. 